Tape Based Magnetic Recording: Technology Landscape Comparisons with Hard Disk Drive and Flash Roadmaps

Robert E. Fontana, Jr.[1], Steven R. Hetzler[2], Gary Decad[1]

[1]Almaden Research Center, IBM Systems Technology Group, San Jose, CA 95120, USA
[2]Almaden Research Center, IBM Research Division, San Jose, CA 95120, USA

This paper describes the areal density (bits per unit area) roadmap goals for tape based magnetic recording (TAPE) and uses these goals as counterpoints for the areal density roadmap strategies for Hard Disk Drive (HDD) and NAND flash. Technology comparisons described in this paper will show that presently volumetric densities (bits per unit volume) for TAPE, HDD, and NAND are similar and that lithographic requirements (the size of minimum device features used to form the bit cells) for TAPE are less challenging than those for NAND and HDD One result of the technology comparison discussion will be that the potential for sustained annual areal density increase rates for TAPE is significantly greater than that for NAND and HDD due to the present TAPE bit cell area and bit cell volume being a factor of 200 – 300 larger than the respective NAND and HDD bit cell area and volume. Larger bit cell area relative to HDD and NAND means that TAPE areal density will increase with minimum dependencies on forming nanoscale features. Larger bit cell valume relative to HDD and NAND means that TAPE areal density will increase with minimum dependencies on bit stability.

***Index Terms*—NAND, HDD, Tape, areal density**

I. Introduction

A measure of the extendibility of storage class memory (SCM) devices, i.e. TAPE Cartridges, Hard Disk Drives (HDD), and Solid State FLASH Drives (SSD) has been areal density, i.e. the number of bits stored per unit area. Projections for areal density increases establish roadmap goals for these technologies. For the last 6 years, TAPE, NAND Flash, and HDD have been characterized by annual areal density increases of 40%. This increase rate implies that over the last six years areal density has increased by a factor of 8X. The premise of this paper is that over the next six years, only TAPE will be able to sustain this rate of areal density increase. As will be described in this paper, the simple conclusion is that since the TAPE bit cell is a factor of 200 to 300 larger than the HDD or NAND Flash bit cell (see Figure 1), the TAPE bit cell is therefore more easily scaled to smaller sizes. TAPE can achieve annual areal density increases that exceed those of both HDD and NAND. The implication of this technology statement is that the mix of future SCM applications requiring volumetric efficiencies will favor TAPE.

II. Areal density History and Roadmaps

A classic measure of technology improvement for SCM

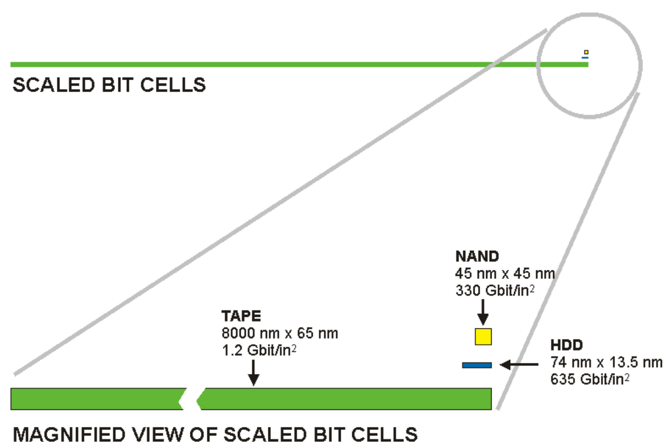

Figure 1. Scaled views of YE2010 bit cells for NAND, HDD, and TAPE

devices is the areal density roadmap. The stated goal for TAPE, HDD, and NAND Flash has been to double areal density every two years, i.e. increase areal density annually by 40%. The desired result for this roadmap is that at the device level, i.e. the cartridge for TAPE, the disk platter for HDD, and the basic NAND Flash chip, capacity doubles within the same volume without increasing cost. SCM users can therefore project future volumetric and cost per bit enhancements. Figure 2 shows a historical perspective of areal density increases for SCM technologies and projects future areal densities assuming a continuation of 40% annual increases.

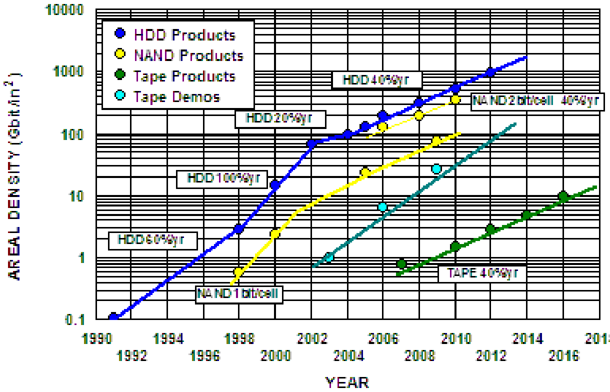

Figure 2. Areal Density History for TAPE, HDD, and NAND Flash

The HDD areal density history is characterized by both growth rates in the 100% to 40% range driven by technology introductions like GMR or giant magneto-resistance sensors in 1998 and perpendicular media in 2004 and TMR or tunneling magneto resistance sensors in 2006 and by growth rates as low as the 20% range between new technology introductions.

The NAND Flash areal density history is also characterized by growth rates in the 100% to 40% range; coming from both changes in the bit cell design in the 1998 time period and in the transition to cell designs that accommodate 2 bits in the 2006 time frame and by improvements in photolithography where feature size is reduced by 15% to 20% annually or bit cell area decrease by 30% to 40% annually. Lithography plays a more critical role in NAND flash over HDD, since the bit cell in NAND flash is defined by lithography in both length and width while in HDD the bit cell is defined by lithography in only one dimension [1, 2].

TAPE areal density history is characterized by consistent growth rates in the 30% to 40% range as documented by the introduction dates of the current Linear Tape Open (LTO) technology five product generations [3]. Tape also is characterized by a set of technology component demonstrations that lay the groundwork for future tape products.

The issue for all three technologies is how to continue areal density rates in the range of 40% as projected in Figure 2.

III. The Bit Cell and Photolithography

Table 1 shows the bit cell dimensions for NAND, TAPE, and HDD first for YE 2010 reported values and then for YE 2014 values assuming 40% / year areal density increases are realized. Figure 3 shows the lithographic projections for NAND flash dimensions as proposed by the International Technology roadmap for Semiconductors (ITRS).

NAND flash bit cells are formed lithographically in both the width and length dimension. Cell area is expressed as $\alpha \times F^2$ where F is the lithographically formed minimum feature. YE2010 NAND bit cells have areas of $3F^2$ with minimum feature F of 0.025 um or 25 nm. NAND Flash has standardized on a 2 bit per cell design so another step increase in areal density like that realized in 2002 (Figure 1) is unlikely since 3 bit per cell (8 states) designs contend with charge retention limiting state endurance. Future areal densities will be achieved almost exclusively with lithography so meeting the 2014 density goals would require minimum features approaching 12 nm (Table 1), a dimension that presently is not on the ITRS lithography roadmap [3] (Figure 2).

Table I. Bit Cell Dimensions for NAND, Tape, and HDD

TECHNOLOGY METRIC	2010	2014 (40% /YR)
TAPE		
-- Areal Density	1.2 Gbit/in^2	4.8 Gbit/in^2
-- Bit Length	8000 nm	2000 nm
-- Bit Width	100 nm	100 nm
-- Minimum Feature	4000 nm	1000 nm
HDD		
-- Areal Density	635 Gbit/in^2	2500 Gbit/in^2
-- Bit Length	74 nm	19 nm
-- Bit Width	13.5 nm	13.5 nm
-- Minimum Feature	37 nm	10 nm
NAND Flash		
-- Areal Density	330 Gbit/in^2	1300 Gbit/in^2
-- Bit Length	45 nm	20 nm
-- Bit width	45 nm	20 nm
-- Minimum Feature	25 nm	12 nm

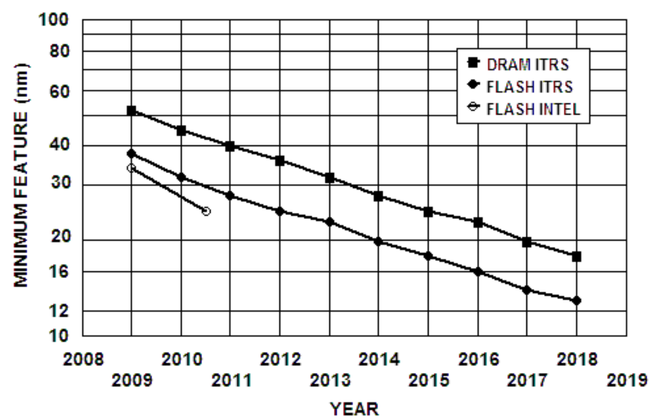

Figure 3: ITRS Lithography roadmap history for semiconductor processing and INTEL/MICRON NAND lithography in benchmarks

A distinguishing feature of HDD and TAPE bit cells is that only one dimension of the bit cell is formed by lithography, i.e. the length while the other dimension is formed electronically and is sub-lithographic in extent. The sub-lithographic nature of one of the dimensions of the HDD bit cell enables greater areal density than NAND flash cells which are constrained by lithography in both dimensions.

HDD and TAPE bit cells are formed lithographically in the length dimension by the lateral dimension of a write pole tip. HDD and TAPE bit cell widths are formed by the distance the magnetic media (tape or disc) moves during the time duration a current pulse into the write head is activated. When the pulse turns off or reverses polarity, a new bit is then written. In essence, the widths of magnetic bits cells are self assembled on the media without the aid of lithography and with the aid on the write field activated by current. For HDD and TAPE the minimum lithographic feature is the lateral dimension of a sensor that detects the bit and not the lateral dimension of the write head. A “write wide / read narrow” strategy is adopted so that the read transducer can successfully be servoed over the written transition or bit cell with high accuracy. This dimension, F, is typically 50% of the lateral track pitch so the lateral track pitch in magnetic recording is 2.0F and the lateral extent of the write transducer is 1.6F and the lateral extent of the read transducer is 1.0F. HDD and Tape magnetic recording bit cells are characterized by an aspect ratio, i.e. a bit aspect ratio or BAR. Typical BARs for HDD bit cells[1,2]. Typical BARs for TAPE bit cells are ~ 7-8. Referring to Table I HDD areal density goals in 2014 will also stress minimum feature processing as is the case with NAND. On the other hand, TAPE minimum features are over a factor of 100 larger in the 2014 time frame due to the large BAR for TAPE bit cells, This suggests that areal density goals will be achieved for TAPE with minimum lithographic impact.

IV. Volumetrics Examples

From a product standpoint, areal density capabilities must be translated into device capacities. Here the true technology metric becomes not only cost per bit but also bit per unit volume. The volumetric requirement is what equalizes the disparity in areal density between HDD and TAPE. The volumetric advantage for NAND is diminished by the cost of the bit. Volumetric comparisons for YE 2010 components are shown in Table II.

Table II. Volumetric Comparisons for HDD, NAND, and TAPE Components (YE 2010)

	SSD (FLASH) Drive	**HDD (DISK) Drive**	**GEN5 (TAPE) Cartridge**
Capacity	0.5 TB	3.0 TB	1.5 TB
Price	$1500	$200	$50
$/GB	$3.00	$0.07	$0.03
Access Time	µ seconds	m seconds	seconds
Components	128 4 GB NAND chips	4 87 mm disk platters	1 tape cartridge (12.5mm x 820 m)
Device Volume	4.2 in^3	24.2 in^3	14.8 in^3
Storage Density	120 GB/ in^3	120 GB/ in^3	101 GB/ in^3

The parameters used in determining the device volumes were a 2.5” disk drive form factor for the NAND Drive, a 3.5” disk drive form factor for the HDD Drive, and a standard Linear Tape Open (LTO) form factor for the tape cartridge. At the YE 2010 time point, reflecting 9 months of Generation 5 tape media, all technologies have comparable volumetric densities, within 20%. Yet as noted in Table I, the areal density of tape is a factor of 200 to 300 smaller than the areal density of NAND Flash and HDD. Tape volumetric efficiency comes from the thickness of the media in comparison with the thickness of a disk substrate or a silicon substrate. Tape media is 6 um thick; disk substrates are 800 um to 1000 um thick, and silicon substrates are 600 um thick but usually thinned during the packaging process down to 250 um range. The prices shown in Table II are approximate and reflect ranges in 4Q 2010. In principle, assuming areal density improves equally, i.e. 40% annual increases for all three SCM technologies, volumetric density for the SCM technologies remains equivalent.

V. Areal Density Assessments for NAND, HDD, and TAPE

Lithography requirements play a major role in assessing future areal density increases for NAND flash, HDD, and TAPE. In addition, investment costs for new technology development in media strategies (patterning, thermal assist) drive HDD areal density increases. Mechanical issues related to flexible media drive TAPE areal density increases.

The “state of the art” NAND devices are 8 GB chips, 166 mm^2 in area, built with 25 nm minimum features using a 2 bit per cell design that yields a cell size of $3F^2$ [5]. Only 73% of the chip area is used for memory cell storage. Figure 4 shows the chip design for an Intel / Micron product. Note the area of the chip not used for memory storage. The local areal density is 330 Gbit/in^2. An assessment of the future of NAND Flash rests on both economics and on technology. Technology addresses the ability to shrink the bit cell size through lithography. As noted in Section III, the 40% per year roadmap goals force NAND to minimum features of 12 nm in the 2014 time period since moving to 3 or 4 bit per cell flash designs are limited by data integrity due to multiple re-write or longevity problems associated with smaller cells. Lithography alone will limit areal density increases in NAND flash and as seen in Figure 3 a likely lithography feature of 16 nm (midway between the ITRS and the INTEL/MICRON projections) would be achievable in the 2014 timeframe.

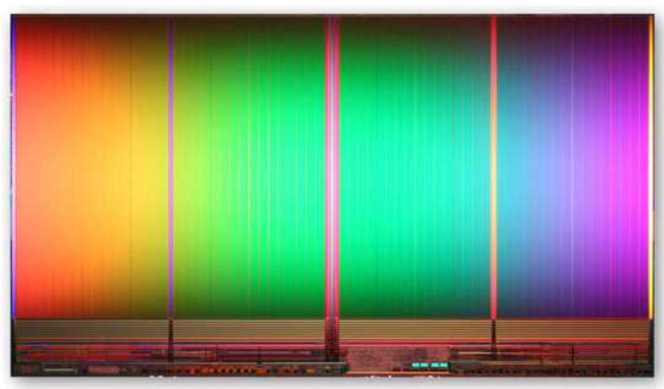

Figure 4. Intel Micron 8 GB NAND flash device, 2 bit per cell, 25 nm minimum feature, 16.5 mm x 10.1 mm [5].

The economics of NAND are driven by basic wafer costs for a 25 mask process of $1500. In 2010 there are 384 8GB chips using 25 nm features on a 300 mm diameter Si wafer today yielding 3 TB per wafer for $500/TB or $0.50/GB just at the wafer level (unpackaged). Contrast this price with the $0.10/GB price for a completed and fully operation hard disk drive. For 2014 with 32 GB chips using 12 nm features yield

12 TB on 300 mm diameter Si wafer at $125/TB or $0.125/GB at the wafer level (unpackaged). In view of ITRS roadmaps alone, a better assessment for the NAND landscape in 2014 would be at best 16 nm features (i.e. an annual reduction in minimum feature of 12% per year rather than an 18% reduction) so scaling wafer capacity for this feature yields at most 8 TB with 24 GB chips and costs of $190/TB.

The HDD landscape has been historically 40% per year increases in areal density. The HDD bit cell is not patterned providing the HDD price per bit a significant, at least 10X, advantage over NAND flash at the component level. All the HDD bit cells (typically > 10^{11}) on a disk surface are magnetically imprinted onto a magnetic disk surface using a **single** lithographically formed write and read structure to define and detect the bit length and using electrical timing of a write current pulse to define the bit width. The aspect ratio of the bits is greater than 1, typically 6:1. This results in bit cell width dimension exceeding lithographic roadmaps (the width is defined by the distance the disk rotates during between current pulses).

Although HDD is advantaged over NAND in processing simplicity, YE 2009 areal densities for HDD were in the 520 Gbit/in2 range and YE 2010 areal densities were 635 Gbit/in² showing a slowing for the first time since the 2001 timeframe of areal density increases to the 20% to 25% range. This slowing is occurring for two reasons. First, the bit cell size for future areal densities is approaching thermal kT fluctuation limits associated with the media grains in the bit cell. Second, the down track width of the bit cell cannot be reduced due to limitations in sensor resolution so bit aspect ratio becomes smaller and the lateral extent of the read and write transducer is approaching the same lithographic limits as the NAND flash cells. As noted in Table IV extending HDD areal densities on a 40% rate, using YE 2009 values would imply 2 TB/in² areal densities in 2014 and with BAR of 2 the minimum features for the read sensor would approach 15 nm with a bit pitch of 7 nm. The ability to have sensor performance at this dimension is unproven.

More critically, future changes in the media, either by patterning to improve bit stability so grains between adjacent bits are isolated or by incorporating lasers in the head structure to thermally assist the writing of higher (i.e. more stable) H_k media, adds substantial cost to the HDD bit. Patterning bits forces HDD to become more "NAND" like by adopting advanced lithographic processing. The economics of this strategy remain to be demonstrated. On the other hand, adding lasers to the head structure as shown in Figure V to write higher H_k media increases head complexity and adds considerable thermal stress to the media but retains the present HDD advantage of limiting bit formation to the minimum feature of the transducer. However, since approximately

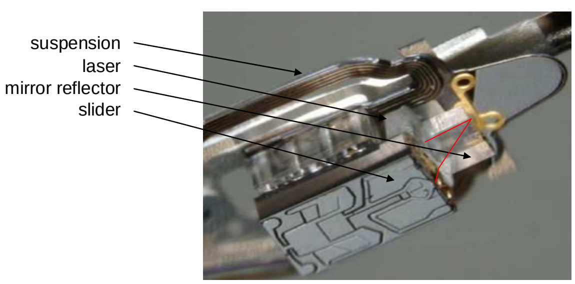

Figure 5. Thermal assist HDD transducer with additional optical components (laser, reflector) from Seagate [6]

2,000,000,000 heads and 2,000,000,000 disk surfaces were produced by the HDD industry in 2010, an immediate transition to patterned media or thermal assist writing will not occur based simply on cost, the number of components, and the surface area of the disks. One can anticipate slowing areal density rates for HDD.

State of the art TAPE is at an areal density of 1.2 Gb/in² with a cartridge capacity of 1.5 TB for 800 m tape length. This areal density is achieved with two 16 track read/write transducers as shown in Figure 6. Over the last 10 years, TAPE's Linear Tape Open (LTO) technology has introduced successive tape products that double areal density every two years, i.e. 40%/yr annual increases [2]. The present areal density in LTO5 products is achieved with a bit cell having a track pitch of 8.1 um and a down track width of 63 nm. The minimum lithographic feature used to detect the bit cells is a read sensor with a 4.0 um lateral extent. These values are contrasted to the state of the art HDD bit cell with a 45 nm read element width and a 13 nm bit width. The factors of 5 in bit width and 100 in bit lateral extent account for the 500X difference in areal density between HDD and TAPE bit cells.

Areal density increases in TAPE are not limited by lithography roadmap issues, even if all of the areal density gains come from improvements in track pitch alone. For example, 40% annual areal density increases over a 4 year period (a 4X increase) would require a sensor width of 1.0 um and an 80% annual areal density increases over the same 4 year period (a 10X increase) would require a sensor width of 0.4 um. A 0.4 um width is still a factor of 10 larger than today's HDD minimum feature.

Figure 6. Read/Write transducer for 16 element tape head

TAPE limitations for areal density increases are not related to "nano" issues associated with lithography or thermal bit stability since the volume of the bit cell is 200X to 500X larger than NAND or HDD bit cells. TAPE limitations come from mechanical realities. First, the thin TAPE media, i.e. the volumetric enhancement for TAPE, is flexible and the ability to track the bit cell location, i.e. servoing, becomes more difficult as the bit length is reduced. Second, the read/write element in contact with the thin media and interactions between the tape and the read head create wear issues that ultimately limit sensor proximity to the media. However, these mechanical issues are identical to the mechanical issues that confront and have been solved by the HDD technology. HDD technology introduced thin overcoats to protect the read sensor from the disk media. Also, HDD technology routinely, on a rigid media, servos to or tracks bits with 0.09 um lateral extent, a dimension significantly smaller than what would be required to track TAPE bits with 1 um track pitches, dimensions needed to sustain 80% areal density growth for tape for the next 4 years.

VI. Areal Density Projections

From the observations in Section V, projections can be made on future areal densities for SCM technologies. These projections are illustrated in Figure 7.

For HDD a reasonable projection is maintaining a 20% annual areal density increase which has been validated by YE2009 and YE2010 reported areal density products. These increases are constrained by four items: lithography requirements for patterned media, operational characteristics for narrow track sensors, media durability for thermal or energy assist writing, and investment costs to transition to novel technologies.

For NAND flash a reasonable projection is also to maintain areal density increases at 20% to 25% annual rates. This is driven by lithography roadmaps. If the ITRS projections of reducing minimum feature by a factor of 2 every 6 years prove valid, then minimum feature reduces by 12% per year or bit area decreases at 23% per year. Novel NAND design changes, i.e. cells supporting 3 or 4 bits (8 or 16 levels) are unlikely since SCM requirements demand bit endurance that to date have not been supported by multiple cell designs.

For TAPE two projections are of interest. First, continuation of the historical annual areal density growth rate of 40% is achievable since no lithographic or bit stability issues impact future areal densities in the next 4 to 6 year time horizon. Second, an even more aggressive annual areal density growth strategy of 80% (10X density increase in 4 years) is appropriate in view of the favorably large bit cell dimensions with such growth. The later increases require improvements, as discussed in Section V, in TAPE media SNR characteristics, in TAPE head servoing to accommodate the smaller trackwidths, and in reducing head to tape separation to increase signal output of the head transducer. Such expertise is however currently practiced in HDD technology.

Using these areal density growth rate projections, Table IV projects device storage capacity and device volumetric storage density in the 2014 time frame (+4 years) for three areal density growth scenarios: 1) continued annual historical growth of 40%, 2) historical growth of 40% for TAPE and reduced 20% growth for HDD and NAND, and 3) aggressive growth of 80% for TAPE and the same reduced 20% growth for HDD and NAND. For reference, 2010 device storage capacity and device volumetric storage density are described in Table II. In particular note that in a 4 year period with HDD and NAND areal density growth rates slowing to 20% coupled with TAPE either sustaining 40% growth or accelerated to 80% growth, then TAPE volumetric storage density improves significantly relative to HDD and NAND volumetric storage density. In particular,within the 2014 time frame for the aggressive 80% TAPE growth areal density scenario, TAPE volumetric density exceeds HDD and NAND volumetric density by a factor of 3 to 4 and TAPE component capacity exceeds HDD and NAND component capacity by a factor of 2

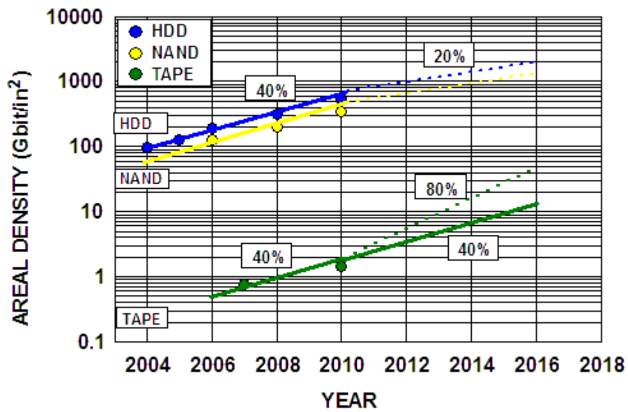

Figure 7. Areal density projections for TAPE, NAND Flash, TAPE

Table IV. 2014 Storage Component Characteristics Based on Areal Density Growth Rate Projections

Areal Density Growth Rates (Qualitative)	**Continued Historical Growth**	**Declining Growth in HDD and NAND**	**Aggressive Growth in Tape**
Areal Density Growth Rates (Specifics)	**2014 40%/yr--TAPE 40%/yr--HDD 40%/yr--NAND**	**2014 40%/yr--TAPE 20%/yr--HDD 20%/yr--NAND**	**2014 80%/yr--TAPE 20%/yr--HDD 20%/yr--NAND**
TAPE			
-- Areal Density	4.8 Gbit/in²	4.8 Gbit/in²	12.0 Gbit/in²
-- Minimum Feature	1.0 um	1.0 um	0.4 um
-- Cartridge Capacity	6.0 TB	6.0 TB	15. 0 TB
-- Volumetric Density	404 GB/in³	404 GB/in³	1000 GB/in³
HDD			
-- Areal Density	2500 Gbit/in²	1300 Gbit/in²	1300 Gbit/in²
-- Minimum Feature	0.010 um	0.018 um	0.018 um
-- HDD Capacity[1]	12.0 TB	6.0 TB	6.0 TB
-- Volumetric Density	480 GB/in³	240 GB/in³	240 GB/in³
NAND Flash			
-- Areal Density	1300 Gbit/in²	700 Gbit/in²	700 Gbit/in²
-- Minimum Feature	0.012 um	0.016 um	0.016 um
-- Chip Capacity	32 GB	24 GB	24 GB
-- SSD Capacity[2]	2 TB	1.2 TB	1.2 TB
-- Volumetric Density	480 GB/in³	300 GB/in³	300 GB/in³

1. 4 -- 87 mm diameter platters in HDD unit
2. Capacity and volumetric density based on 62 mm form factor HDD volume

.

VII. Conclusions

In summary, areal density growth rate scenarios for three SCM technologies, TAPE, HDD and NAND, have been described. These scenarios suggest that TAPE annual areal density growth rates will be either maintained at traditional 40% values or exceed traditional growth rates and approach 80% values. These scenarios also suggest that HDD and NAND annual growth rates will not maintain the traditional 40% values and will rather slow to 20% values. Essentially, the TAPE bit cell is 300X to 500X larger than the HDD and NAND bit cells and hence scalable to smaller areas without being impacted by nano-technology issues related to lithography and bit stability. The net result of these areal density scenarios is volumetric and total capacity storage advantages for TAPE technology over HDD and NAND technologies.

VIII. References

[1] R. Fontana, S. Hetzler, "Magnetic memory devices: minimum feature and memory hierarchy discussion", Journal of Appl. Physics, Vol. 99, No. 8, Part III, pp. 08N901-1 – 08N901-6, April 2006

[2] R. Fontana, N. Robertson, S. Hetzler, "Thin film processing realities for Tbit/in² recording", IEEE Transactions on Magnetics, vol. 44, no. 11, pp. 3617-3620, 2008

[3] LTO Roadmap History, www.lto.org

[4] 2010 ITRS Lithographic Projections, www.itrs.org

[5] Intel Product Description, www.techztalk.com/techwebsite/05-18-10-intel-starts-mass-production-of-25nm-8gb-nand-flash-chip

[6] M. Re, "Has HAMR reached a critical mass", The Information Storage Industry Consortium Symposium on Alternative Storage Technologies, April 2009, www.insic.org